**Department of Computer Engineering**

BLG 242E  
Digital Circuits Laboratory Experiment Report

Experiment : 7 Sequential Logic Circuits

Experiment Date : 22.04.2016

Group Number : 11

Group Members :

|  |  |  |
| --- | --- | --- |
| **ID** | **Name** | **Surname** |
| 150140044 | Doğay | Kamar |
| 150140031 | Pelin | Hakverir |
| 150140051 | Mertcan | Yasakçı |
|  |  |  |

Laboratory Assistant : Nagehan Ilhan

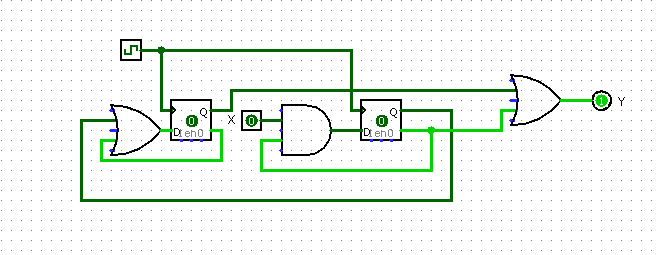
# Introduction

The purpose of this experiment is to implement and analyze sequential logic circuits with finite state machine model.

# Requirements

## part 1

We implemented the circuit as shown below:



The circuit is implemented with:

-74xx08 – Quadruple 2-input Positive AND Gates

-74xx32 – Quadruple 2-input Positive OR Gates

-74xx174 – Hex D-Type Flip-Flops

Firstly, the circuit is a Moore model finite state machine because the output depends only on the current state. Our analysis steps:

Q1+Q0+

|  |  |  |  |
| --- | --- | --- | --- |
| **Q1Q0/X** | **0** | **1** | **Z** |
| **00** | 01 | 11 | 0 |
| **01** | 00 | 10 | 1 |
| **11** | 01 | 01 | 0 |
| **10** | 01 | 01 | 0 |

00=A 01=B

11=C 10=D

|  |  |  |
| --- | --- | --- |
| **Q1Q0/X** | **0** | **1** |
| **A** | 0 | 1 |
| **B** | 0 | 1 |
| **C** | 0 | 0 |
| **D** | 0 | 0 |

|  |  |  |
| --- | --- | --- |
| **Q1Q0/X** | **0** | **1** |
| **A** | 1 | 1 |
| **B** | 0 | 0 |
| **C** | 1 | 1 |
| **D** | 1 | 1 |

D0(Q0+)

D1(Q1+)

D0=Q0’+Q1 D1=X.Q1’ Q0+=D0 Q1+=D1 Y=Q0.Q1’

0

0

1

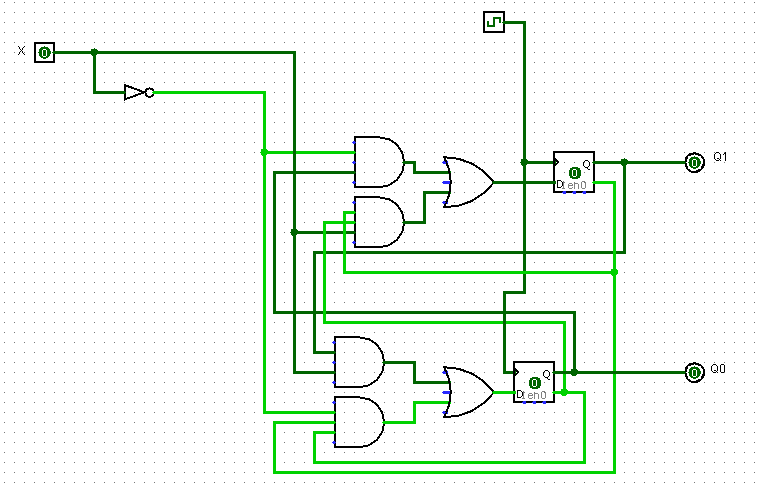
1

0, 1

0, 1

## part 2

We implemented the circuit as shown below:



When X is 0, the circuit counts from 00 to 10 and restarts to count from 00, otherwise, it counts backwards starting from 10 to 00 and restarts to count from 10.

The circuit is implemented with:

-74xx04 – Hex Inverters

-74xx08 – Quadruple 2-input Positive AND Gates

-74xx32 – Quadruple 2-input Positive OR Gates

-74xx174 – Hex D-Type Flip-Flops

Our design steps:

X=1

X=0

X=0

X=0

X=1

X=1

D0(Q0+)

D1(Q1+)

Q1+Q0+

|  |  |  |
| --- | --- | --- |
| **Q1Q0/X** | **0** | **1** |
| **00** | 01 | 10 |
| **01** | 10 | 00 |
| **11** | XX | XX |
| **10** | 00 | 01 |

|  |  |  |
| --- | --- | --- |
| **Q1Q0/X** | **0** | **1** |
| **00** | 0 | 1 |
| **01** | 1 | 0 |
| **11** | X | X |
| **10** | 0 | 0 |

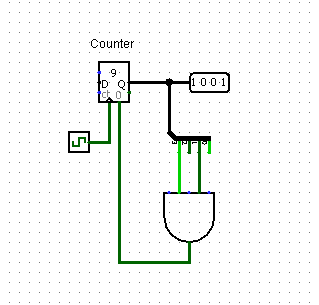
|  |  |  |
| --- | --- | --- |
| **Q1Q0/X** | **0** | **1** |
| **00** | 1 | 0 |
| **01** | 0 | 0 |
| **11** | X | X |
| **10** | 0 | 1 |

D1=Q1.X’+Q1’.Q0’.X D0=Q0.X+Q1’.Q0’.X’

After we implemented the circuit correctly, we checked its behaviour for the undetermined state Q1Q0=11. Firstly we disconnected the flip flops, loaded them with 1, sent the clock signal and reconnect them to the circuit, its behaviour was going to state 10.

## part 3

We implemented the circuit as shown below:



The circuit counts to 9, until the AND product becomes one, in which the second and fourth bits of the result should be 1. That occurs first when the output is 10, and it immediately resets when the counter hits 10.

The circuit is implemented with:

-74xx08 – Quadruple 2-input Positive AND Gates

-74xx161 – Synchronous 4-bit Binary Counter

# Conclusion